

ABSTRACT OF THE DISCLOSURE

When both the sourcing command and the sinking command to the phase comparator are high, the charge pump phase detector creates a high impedance output dead period, which is undesirable. The dead zone can be minimized by resetting the phase comparator when both sourcing command and sinking command are high. Accurate timing of the reset signal is crucial to good PLL phase noise performance and also to the elimination of the dead zone problem. In our invention, accurate reset timing is achieved by including the charge pump delay time caused by the input gate capacitance of the output complementary MOSFETs in the reset signal path.

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